CLAIMS

What is claimed is:

1. A semiconductor device assembly, comprising:

a first semiconductor device;

discrete conductive elements extending over portions of an active surface of said first semiconductor device; and

a second semiconductor device positioned at least partially over said first semiconductor device and resting upon said discrete conductive elements in electrical isolation therefrom.

2. The semiconductor device assembly of claim 1, further comprising a substrate to which said first semiconductor device is secured.

3. The semiconductor device assembly of claim 2, wherein said substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

4. The semiconductor device assembly of claim 1, wherein said discrete conductive elements comprise at least one of bond wires, tape-automated bond elements, and thermocompression bonded leads.

5. The semiconductor device assembly of claim 1, further comprising:

a dielectric coating on at least portions of said discrete conductive elements and electrically isolating at least said portions of said discrete conductive elements from a back side of said second semiconductor device.

6. The semiconductor device assembly of claim 5, wherein said dielectric coating comprises at least one of a nonconductive oxide and a polymer.

7. The semiconductor device assembly of claim 1, further comprising:

a dielectric coating on at least portions of a back side of said second semiconductor device and electrically isolating said second semiconductor device from at least portions of discrete conductive elements adjacent thereto.

8. The semiconductor device assembly of claim 7, wherein said dielectric coating comprises at least one of a nonconductive oxide and a nonconductive polymer.

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9. The semiconductor device assembly of claim 1, further comprising:

an adhesive element between said first and second semiconductor devices.

10. The semiconductor device assembly of claim 9, wherein said adhesive element substantially encapsulates at least portions of said discrete conductive elements located between said first and second semiconductor devices.

11. The semiconductor device assembly of claim 1, further comprising:

at least one additional semiconductor device positioned over said second semiconductor device.

12. The semiconductor device assembly of claim 1, further comprising:

encapsulant material covering at least a portion of at least one of said second semiconductor device, said first semiconductor device, and said substrate.

13. A multi-chip module, comprising:

a substrate including contact areas;

a first semiconductor device comprising bond pads in communication with corresponding contact areas of said substrate by way of discrete conductive elements extending therebetween; and

at least one second semiconductor device positioned at least partially over said first semiconductor device, a back side of said at least a second semiconductor device contacting and electrically isolated from said discrete conductive elements.

14. The multi-chip module of claim 13, further comprising:
an adhesive element positioned between said first semiconductor device and said at least a second semiconductor device.

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15. The multi-chip module of claim 14, wherein said adhesive element substantially laterally surrounds at least portions of said discrete conductive elements located between said first semiconductor device and said second semiconductor device.

16. The multi-chip module of claim 13, further comprising:
a dielectric coating on at least portions of said discrete conductive elements in contact with said backside of said at least one second semiconductor device.

17. The multi-chip module of claim 13, further comprising:
a dielectric coating on at least portions of said back side of said at least one second semiconductor device in contact with said discrete conductive elements.

18. The multi-chip module of claim 13, wherein said substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

19. The multi-chip module of claim 13, wherein said discrete conductive elements comprise at least one of bond wires, tape-automated bond elements, and thermocompression bonded leads.

20. The multi-chip module of claim 13, wherein each of said discrete conductive elements comprises a lead.

21. The multi-chip module of claim 13, further comprising:
an encapsulant material surrounding at least portions of said first semiconductor device and said at least a second semiconductor device.

22. The multi-chip module of claim 13, further comprising:
external connective elements on said substrate coupled to said contact areas.

23. A method for assembling semiconductor devices, comprising:
providing a first semiconductor device;
placing discrete conductive elements over portions of said first semiconductor device; and
positioning a second semiconductor device at least partially over said first semiconductor device and contacting at least some of said discrete conductive elements with a backs ide of said second semiconductor device.

24. The method of claim 23, wherein said positioning said second semiconductor device comprises positioning said second semiconductor device on said at least some of said discrete conductive elements with said back side and said discrete conductive elements in mutual electrical isolation.

25. The method of claim 24, further comprising:
providing a dielectric coating on at least portions of said discrete conductive elements.

26. The method of claim 25, wherein said providing comprises forming at least one of a dielectric oxide and a dielectric polymer coating on at least said portions of said discrete conductive elements.

27. The method of claim 24, further comprising:
forming a dielectric layer on at least portions of said back side.

28. The method of claim 27, wherein said forming is effected prior to said positioning said second semiconductor device.

29. The method of claim 23, further comprising:
applying a quantity of adhesive material to at least an active surface of said first semiconductor device.

30. The method of claim 29, further comprising:
drawing said second semiconductor device toward said first semiconductor device.

31. The method of claim 30, wherein said drawing is effected by at least one of capillary action of said adhesive material, curing of said adhesive material, application of heat to said adhesive material, and vibration of said adhesive material.

32. The method of claim 29, wherein said applying includes applying said quantity of adhesive material to said back side of said second semiconductor device.

33. The method of claim 29, wherein said applying is effected after said positioning said second semiconductor device.

34. The method of claim 33, further comprising:
drawing said second semiconductor device toward said first semiconductor device.

35. The method of claim 34, wherein said drawing is effected during curing of said adhesive material.

36. The method of claim 29, wherein said applying is effected before said positioning said second semiconductor device.

37. The method of claim 36, further comprising:
biasing at least one of said first and second semiconductor devices toward the other of said first and second semiconductor devices.

38. The method of claim 37, further comprising:
controlling said biasing.

39. The method of claim 38, wherein said controlling said biasing comprises controlling biasing force to a level insufficient to deform, kink, bend, or collapse said discrete conductive elements.

40. The method of claim 23, further comprising:
securing said first semiconductor device and a substrate to one another.

41. The method of claim 40, wherein said placing said discrete conductive elements comprises securing said discrete conductive elements to contact areas of said substrate and bond pads of said first semiconductor device.

42. The method of claim 41, wherein said securing comprises electrically connecting bond pads of said second semiconductor device to corresponding contact areas of said substrate.

43. The method of claim 42, further comprising:
encapsulating at least a portion of at least one of said substrate, said first semiconductor device, and said second semiconductor device.

44. The method of claim 42, further comprising:
forming external conductive elements on said substrate in electrical communication with corresponding contact areas.

45. (Amended) A method for assembling semiconductor devices in a stacked arrangement with the stacked arrangement having a height substantially equal to combined thicknesses of each of the semiconductor devices and distances discrete conductive elements associated therewith protrude above said each of the semiconductor ~~device~~devices, comprising:

providing a first semiconductor device with discrete conductive elements protruding from an active surface thereof; and

positioning a second semiconductor device at least partially over said first semiconductor device and on at least some of said discrete conductive elements such that said back side and said at least some of said discrete conductive elements are electrically isolated from each other.

48. (Amended) The method of claim 46, ~~further comprising:~~ ? typo

~~forming~~wherein said positioning comprises positioning a second semiconductor device that includes a dielectric coating on at least portions of said back side thereof.

45. A method for assembling semiconductor devices in a stacked arrangement with the stacked arrangement having a height substantially equal to combined thicknesses of each of the semiconductor devices and distances discrete conductive elements associated therewith protrude above each semiconductor device, comprising:

providing a first semiconductor device with discrete conductive elements protruding from an active surface thereof; and

positioning a second semiconductor device at least partially over said first semiconductor device and on at least some of said discrete conductive elements.

46. The method of claim 45, wherein said positioning comprises positioning said second semiconductor device on said at least some of said discrete conductive elements with a back side of said second semiconductor device electrically isolated from said discrete conductive elements.

47. The method of claim 46, further comprising:

providing a dielectric coating on at least portions of said at least some of said discrete conductive elements.

48. The method of claim 46, further comprising:

forming a dielectric coating on at least portions of said back side.

49. The method of claim 45, further comprising:

applying a quantity of adhesive material at least to said active surface of said first semiconductor device.

50. The method of claim 49, further comprising:

drawing said second semiconductor device toward said first semiconductor device.

51. The method of claim 50, wherein said drawing is effected by at least one of capillary action of said adhesive material, curing of said adhesive material, application of heat to said adhesive material, and vibration of said adhesive material.

52. The method of claim 49, wherein said applying is effected before said positioning.

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53. The method of claim 49, wherein said applying is effected after said positioning.

54. The method of claim 53, further comprising:
drawing said second semiconductor device toward said first semiconductor device.

55. The method of claim 54, wherein said drawing is effected during curing of said adhesive material.

56. The method of claim 49, further comprising:
biasing at least one of said first and second semiconductor devices toward the other of said first and second semiconductor devices.

57. The method of claim 56, further comprising:
controlling said biasing.

58. The method of claim 57, wherein said controlling said biasing comprises controlling biasing force to a level insufficient to deform, kink, bend, or collapse said discrete conductive elements.

59. The method of claim 45, further comprising:
positioning said first semiconductor device relative to a substrate.

60. The method of claim 59, further comprising:

connecting said discrete conductive elements to corresponding contact areas of said substrate.

61. The method of claim 59, further comprising:
establishing electrical communication between bond pads of said second semiconductor device and corresponding contact areas of said substrate.

62. The method of claim 61, wherein said establishing communication comprises:
placing additional discrete conductive elements between each of said bond pads and a corresponding contact area of said corresponding contact areas.

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63. The method of claim 46, further comprising:
providing at least one external connective element in communication with at least one bond pad of each of said first and second semiconductor devices.

64. The method of claim 63, further comprising:
encapsulating at least portions of said first and second semiconductor devices.

65. A semiconductor device assembly, comprising at least two semiconductor devices in a stacked arrangement, said stacked arrangement having a height substantially equal to combined thicknesses of said at least two semiconductor devices and distances discrete conductive elements associated therewith protrude above each semiconductor device of said at least two semiconductor devices.

66. The semiconductor device assembly of claim 65, wherein said discrete conductive elements comprise bond wires.

67. The semiconductor device assembly of claim 65, wherein a back side of each upper semiconductor device of said at least two semiconductor devices rests upon upper portions of discrete conductive elements protruding above a surface of a next lower semiconductor device of said at least two semiconductor devices.

68. The semiconductor device assembly of claim 65, further comprising:

a substrate to which at least one semiconductor device of said at least two semiconductor devices is secured, said height of said stacked arrangement including a thickness of said substrate.

69. The semiconductor device assembly of claim 35, further comprising:

a protective encapsulant surrounding portions of at least one of said at least two semiconductor devices, said height of said stacked arrangement including a thickness of said protective encapsulant over a surface of at least one of said at least two semiconductor devices.